REMARKS AND ARGUMENTS

Rejections to the claims under 35 USC § 103

Claims 1-6, 23-24 and 31-34 are rejected under 35 USC § 103(a) as being unpatentable over US Patent No. 6,049,220 (*Borden*) in view of US Patent No. 6,022,750 (*Akram et al.*). Applicant respectfully disagrees.

Independent claim 1 has been amended to more clearly recite the invention. As amended, it recites a test method which comprises providing first, second and third test structures on a wafer each having respective first, second and third test structure parameters. At least one test measurement is obtained from each of the test structures. A goodness of fit value is calculated by evaluating the difference between predicted values and test measurement values obtained. The goodness of fit value is used to monitor processes used to form a device. Independent claim 23, similar to claim 1, also requires first, second and third test structures on a substrate and calculating a goodness of fit value which is based on an evaluation of difference between predicted values and test parameter values measured.

Borden describes a method for evaluating a wafer. The method measures a property that is affected by charge carriers present in doped regions of a wafer. A profiler measures intensity of reflected probe beams from the surface of the wafer in the doped regions. Intensity measurements from a wafer with unknown properties (target wafer) are compared with those of wafers with known properties (reference wafers) to determine the properties of the target wafer. *See Borden*, col. 20, line 50 – col. 21, line 35

Akram et al. describes an interconnect for a semiconductor die that includes test structures. The interconnect is provided between the die and a temporary package base to establish electrical communication between the package base and die.

The Examiner admits that *Borden* fails to teach or describe the limitation of first, second or third test structures each having respective first, second and third test structure parameters. To compensate for this defect, the Examiner relies on *Akram et al.* Applicant submits that there is no suggestion to combine the references as suggested by the Examiner.

It is well established that there must be a reason, suggestion, or motivation from the prior art as a whole for the person of ordinary skill to have combined or modified the references. *See, e.g., In re Geiger*, 815 F.2d 686, 2 USPQ 2d 1276 (Fed. Cir. 1987). Absent such incentives, the references are not combinable. *See Ex parte Skinner*, 2 USPQ 2d 1788 (B.P.A.I 1987). Furthermore, it is impermissible to use the claimed invention as an instruction manual or template to piece together the teachings of the prior art so that the claimed invention is rendered obvious. *See In re Fitch*, 972 F.2d 1260, 23 USPQ 2d 1780 (Fed. Cir. 1992).

As discussed, Borden measures reflectance of the doped wafer region using probe beams. No test structures are used or discussed in Borden. It is not understood how one of ordinary skill in the art would combine the test structures of *Akram et al.* with *Borde*. In fact, Applicant submits that one would not use test structures on the wafer above its surface since they would interfere with the intensity measurements of the probe beams reflected. As such, Borden teaches away from the presently claimed invention of using test structures.

Even assuming that there is a suggestion to combine the references, this would still fail to teach or suggest the claimed invention. As claimed, the test structures are on the wafer. On the other hand, the test structures of *Akram et al* are located on an interconnect which is external to the die (or wafer). At best, the combination of reference would suggest external test structures, not test structures on the wafer as claimed.

Moreover, in rejecting the claims, the Examiner indicated that Borden teaches calculating a goodness of fit value which is used to monitor processes used to form said device. However, Applicant's review of Borden, including the sections referred to by the Examiner, failed to find

any mentioning of calculating a goodness of fit value as claimed. Furthermore, claim 1 requires that the goodness of fit value is calculated based on an evaluation of difference between predicted values and test measurement values obtained. On the other hand, Borden compares test measurements from a target wafer to those of reference wafers. Borden nowhere teaches the use of predicted values. Applicant therefore submits that for at least the above discussed reasons, claims 1 and 23 and their directly or indirectly dependent claims are patentable over *Borden* and *Akram et al.*, alone or in combination.

Claim 30 is rejected under 35 USC §103(a) as being unpatentable over *Borden* in view of US *Akram et al.* and further in view of US Patent No. 5,787,190 (*Peng et al.*). Applicant respectfully disagrees.

Claim 30 is dependent on claim 1. As already discussed, claim 1 is patentable over *Borden* and *Akram et al.*, alone or in combination. The addition of *Peng et al.*, which the Examiner relies on to teach obtaining test measurement values from two or more test sites, fails to compensate for the defects of *Borden* and *Akram et al.* As such, Applicant submits that claim 31 is patentable over B*orden, Akram et al.* and *Peng et al.*, alone or in combination.

Claims 25 and 26 are rejected under 35 USC §103(a) as being unpatentable over *Borden* in view of US Patent No. 7,091,733 (*Takekoshi et al.*). Applicant respectfully disagrees.

Claim 25, similar to claim 1, recites providing a device structure on a wafer having a plurality of first test structures with respective test structure parameters on a wafer. First, second and third test measurements are measured form at least one of the test structures and a goodness of fit value is calculated based on evaluation of the difference between predicted values and test measurement obtained.

As already discussed with respect to claim 1, *Borden* fails to teach or suggest forming a plurality of test structures on a wafer having respective test structure parameters as well as calculating a goodness of fit value based on an evaluation of the difference between predicted

values and test measurement obtained. The Examiner relies on *Takekoshi et al.* to teach measuring second and third test measurement on at lest the first test structure. Even if this were the case, Applicants submit that *Takekoshi et al.* fails to compensate for the defects of Borden. Applicant therefore submits that claims 25 and 26, which depends from claim 25, are patentable over *Borden* and *Takekoshi et al.*, alone or in combination.

With respect to newly added clam 35, it recites a method of forming a device. Similar to claim 1, claim 35 requires test structures on a wafer with respective test structure parameters as well as determining a goodness of fit value based on an evaluation of the difference between predicted values and test measurement values obtained. For similar reasons already presented with respect to claims 1, 23 and 25, newly added claim 35 is also patentable over relied the upon references, alone or in combination.

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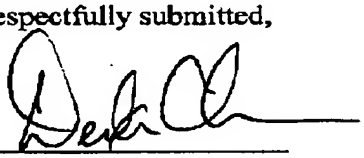
Conclusion

It is respectfully submitted that this application is in condition for allowance and the issuance of a formal Notice of Allowance at an early date is respectfully requested. Should the Examiner believe that a telephone conference would expedite prosecution of this application, please telephone the undersigned attorney at his number set out below.

Date: March 14, 2008

Respectfully submitted,



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